Operation of the new 256 MPPC array with BGO

Goals:

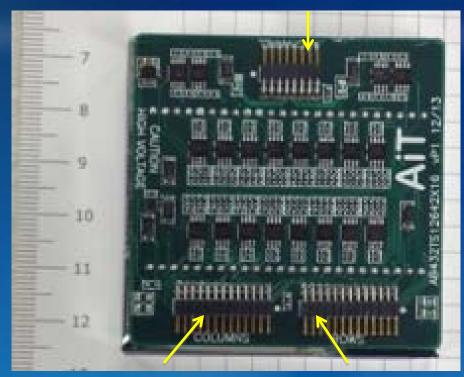
- Separate at least 2mm BGO pixels @ 511 keV
- Achieve 15% FWHM @ 511 keV
- Added requirement: Obtain simple DOI scheme with stacked arrays
- Consider cooling if necessary to achieve the above goals





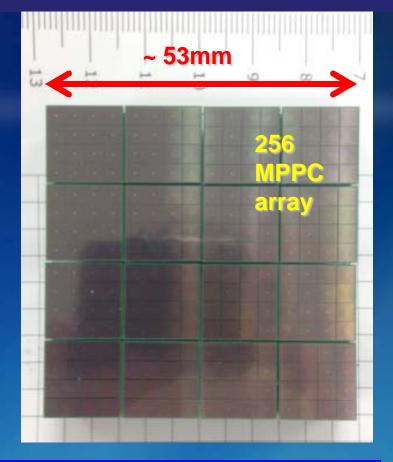
Studies with 16x16 MPPC array with 2mm BGO array

4ch readout



16ch columns 16ch rows

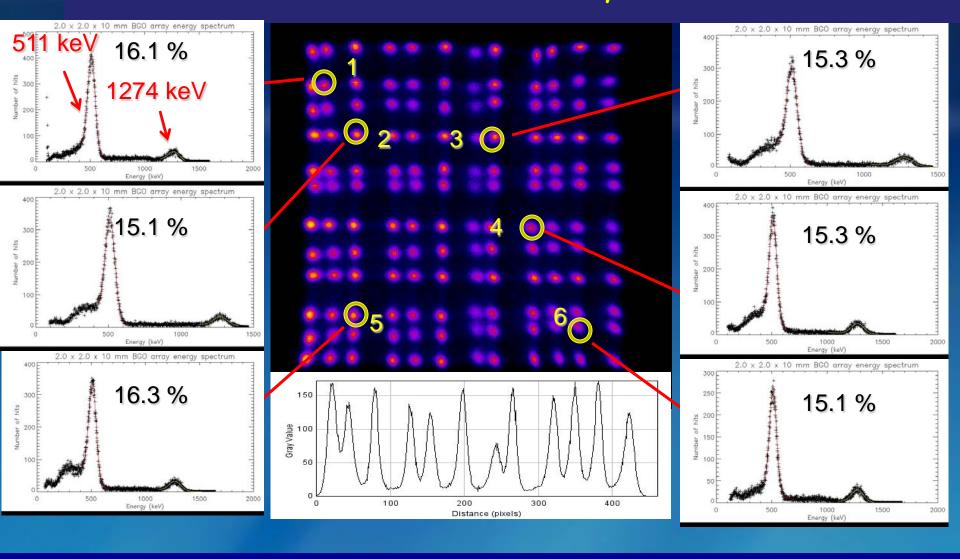
Hybrid readout board from AiT Instruments with the row-and-column outputs and a 4ch output



This prototype of the 256 MPPC array was assembled by AiT Instruments as an array of sixteen model **512642-050CN-9(X)** modules, each with 16 MPPCs.

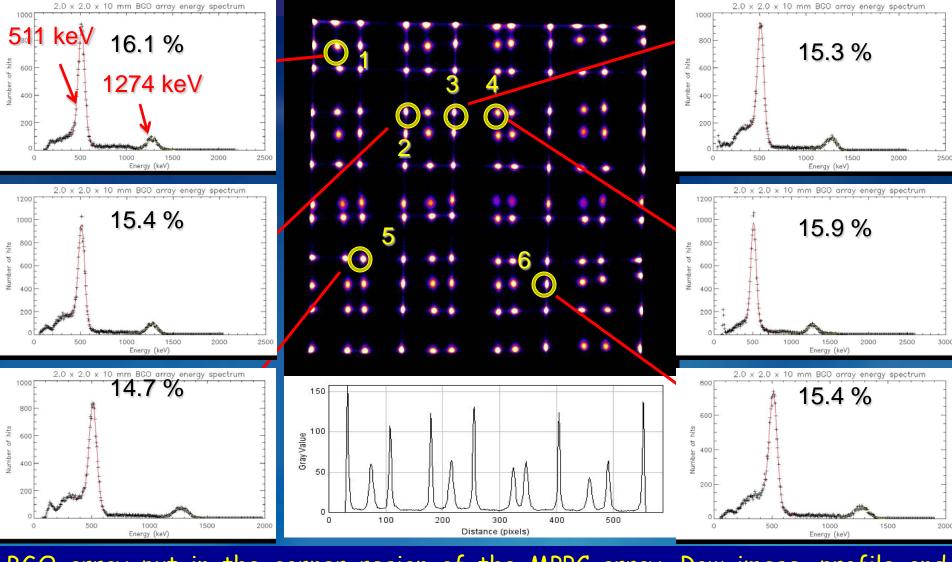
256 element MPPC array was tested with a 2x2x15 mm BGO array from Proteus coupled directly, without an additional window, to the MPPC array. Visilox V-788 optical coupling compound was used between the MPPC array and the BGO array.

12x12 2x2x15mm BGO array, 4ch readout



Row image, profile and examples of six energy spectra from six BGO pixels. FWHM energy resolution values (%) at 511 keV. (Temp = 14.4 deg C. V= 67.2 V, 1000ns ADC integration gate. F factor 0.05. BGO array put in the corner region of the MPPC array. 4ch readout.)

12x12 2x2x15mm BGO array, 16x16ch readout



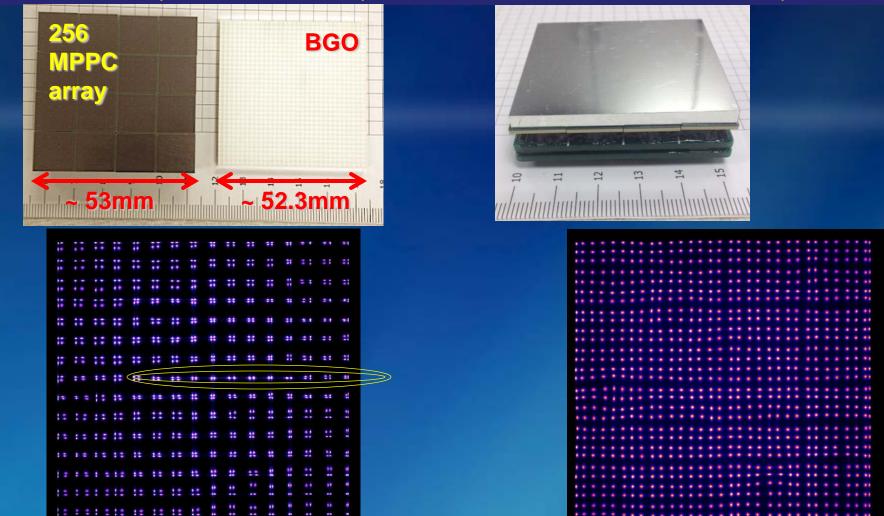
BGO array put in the corner region of the MPPC array. Row image, profile and examples of six energy spectra from six BGO pixels. FWHM energy resolution values (%) at 511 keV. (Temp = $14.4 \, \text{deg} \, \text{C}$. V= $67.2 \, \text{V}$, $1000 \, \text{ns} \, \text{ADC}$ integration gate. F factor 0.025. Row-and-column readout.)

Summary of the pilot 2mm BGO array studies with the 256 MPPC module

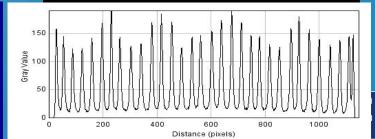
| • | Bias | _ | gate width | | | | | | |
|---------|------|---------|---------------|-------|-------|-------|-------|-------|-------|
| (deg C) | (V) | Readout | (ns) | roi_1 | roi_2 | roi_3 | roi_4 | roi_5 | roi_6 |
| 23.0 | 67.8 | 4ch | 500 | 14.5 | 17.9 | 17.4 | 17.8 | 16.5 | 17.0 |
| 23.0 | 67.8 | 4ch | 1000 | 15.1 | 17.8 | 16.1 | 15.9 | 16.4 | 15.0 |
| 23.0 | 67.8 | 16x16ch | 500 | 16.5 | 16.8 | 17.9 | 17.2 | 17.7 | 17.4 |
| 23.0 | 67.8 | 16x16ch | 1000 | 17.9 | 15.8 | 16.9 | 17.6 | 15.4 | 16.9 |
| 14.4 | 67.2 | 4ch | 1000 | 16.1 | 15.1 | 15.3 | 15.3 | 16.3 | 15.1 |
| 14.4 | 67.2 | 16x16ch | 1000 | 16.1 | 15.4 | 15.3 | 15.9 | 14.7 | 15.4 |
| 14.4 | 67.2 | 4ch | 500 | 17.1 | 16.2 | 16.6 | 17.4 | 17.3 | 16.8 |

Table of FWHM energy resolution values (%) at 511 keV. The best performance was obtained at 14.4 deg C with 1000 ns ADC integration gate.

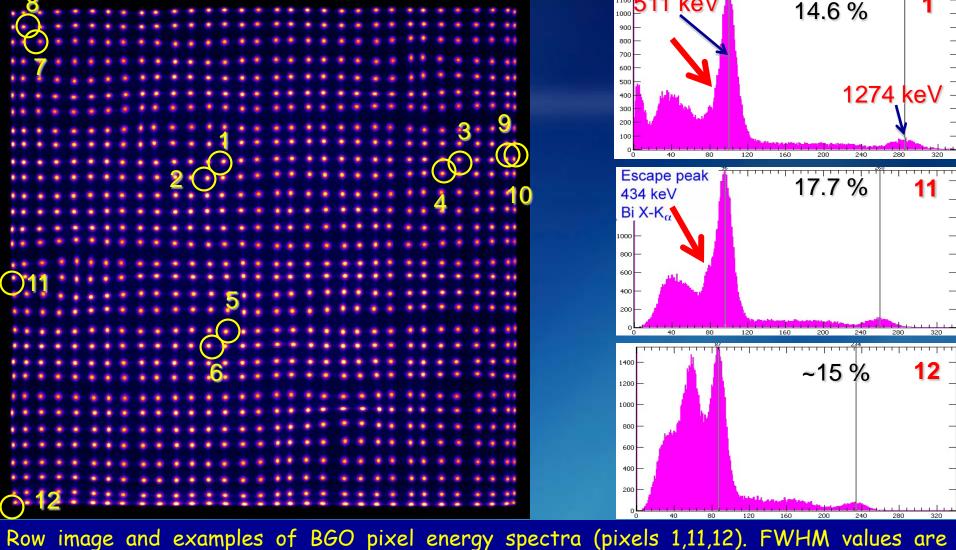
32x32 pixel 1.63mm pitch x 3mm thick BGO array



Row images obtained with the direct coupling of the BGO array to the MPPC array (left), and with the additional 1.2mm thick spreader window (right). Without window, the pixels merge in the cracks between the 16ch modules. Optical grease used on all optical joints.

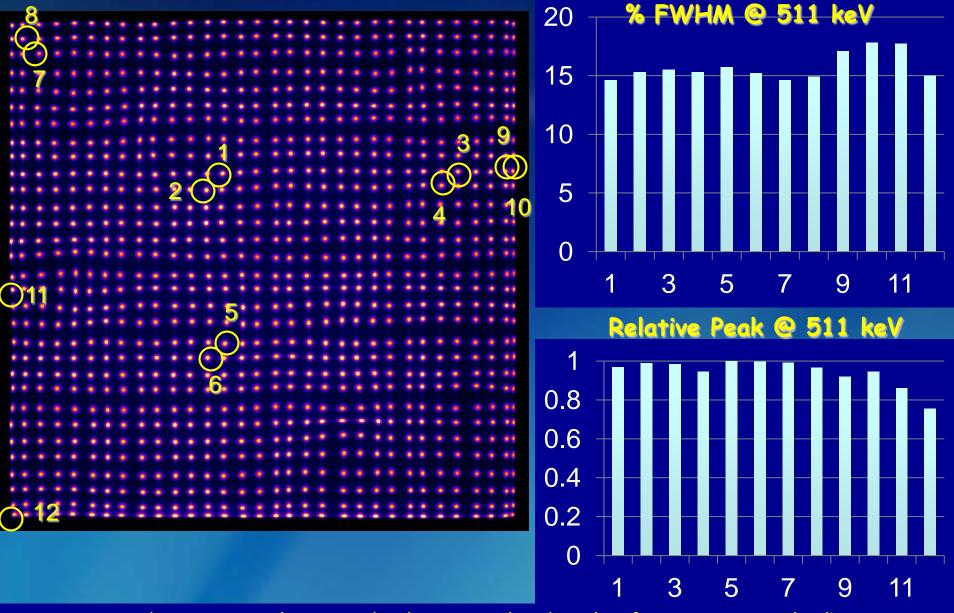


32x32 pixel 1.63mm pitch x 3mm thick BGO array



provided for the 511 keV photopeaks. The red arrows indicate contributions to the photopeaks from the escape 434 keV peak. 1274 keV photopeaks were used to correct for energy shift present when using the diode-based readout circuitry. (Temp = 15.0 deg C. V= 67.2 V, 1000ns ADC integration gate. F factor 0.025. Row and column readout.)

32x32 pixel 1.63mm pitch x 3mm thick BGO array



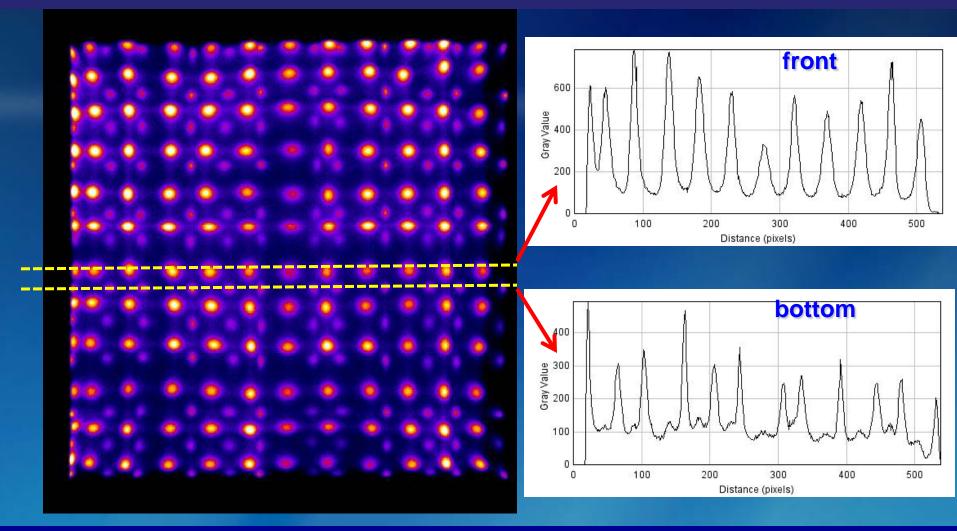
Row image and energy resolution and relative amplitude vales for 12 BGO pixels. (Temp = 15.0 deg C. V= 67.2 V, 1000ns ADC integration gate. F factor 0.025. Row and column readout.)

Stack of two 12x12 2x2x15mm BGO arrays, 16x16ch readout



BGO array stack put in the center of the MPPC array. The bottom 2mm array shifted by 1mm in both planar x-y coordinates relative to the top one. Scintillation light from the top array reaches MPPC array through the bottom array that is optically open on both sides.

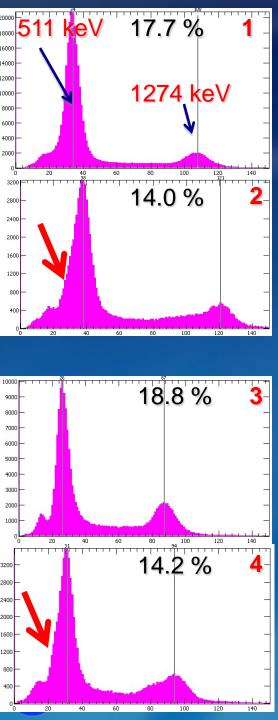
Stack of two 12x12 2x2x15mm BGO arrays, 16x16ch readout



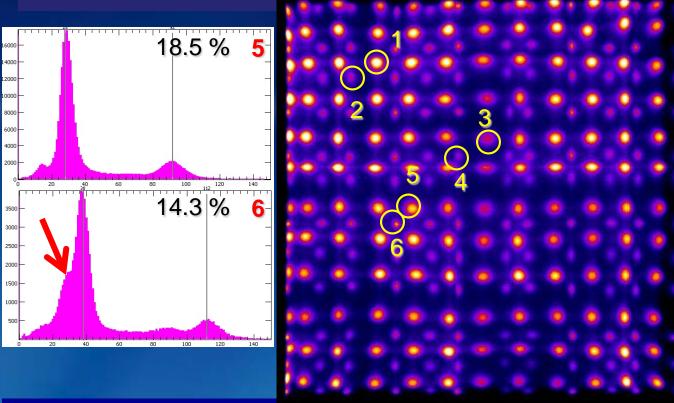
Row image and two profiles through the front (top) and back (bottom) arrays at 511 keV. All pixels separate well. (Temp = 16.9 deg C. V= 67.2 V, 1000 ns ADC integration gate. F factor 0.025. Row and column readout.)





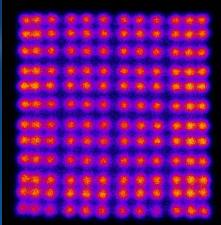


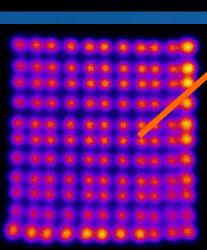
Stack of two 12x12 2x2x15mm BGO arrays

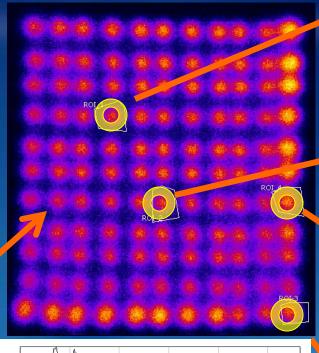


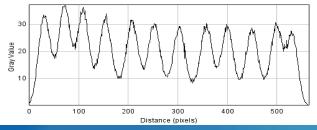
Row image and examples of six energy spectra: three from the front (top) and three from the back (bottom) pixels. FWHM values are provided for the 511 keV photopeaks. The red arrows indicate contributions to the photopeaks in the back layer with less than 511 keV energy deposit due to scattered gammas from layer 1. Energy resolutions in layer 2 pixels were estimated after subtraction of this contribution. 1274 keV photopeaks were used to correct for energy shift present when using the diode-based readout circuitry. (Temp = 16.9 deg C. V= 67.2 V, 1000ns ADC integration gate. F factor 0.025. Row and column readout.)

Reference: Studies with H8500 PSPMT



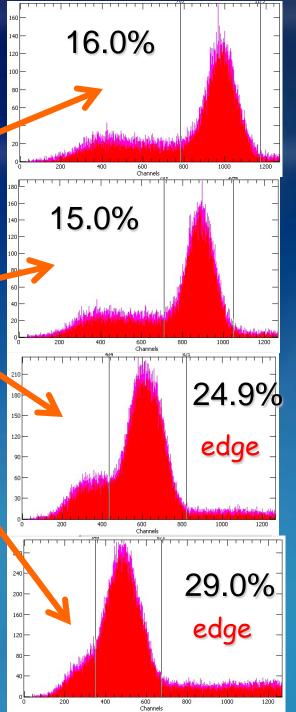






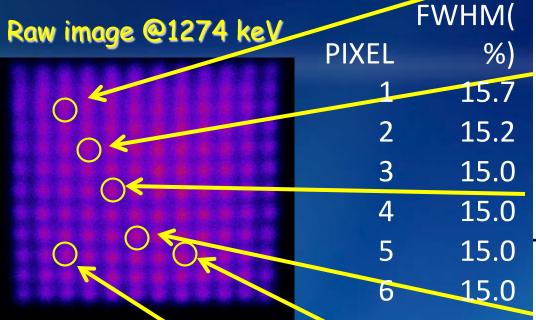
Raw images at left for the central (top image) and corner (bottom image) locations of the 2x2x15mm BGO array.

FWHM energy resolution @511 keV indicated next to the four spectra. Plot for one of the pixel rows in the center.

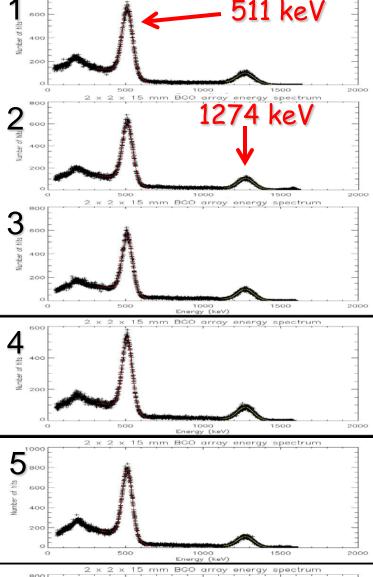


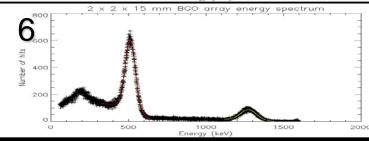


Reference: H8500 PSPMT + 2x2x15mm BGO array with NIM electronics



To confirm performance limit, post-amplifier system was implemented with spectroscopic EG&G/Ortec amplifiers (such as model 572). I microsecond shaping was applied to pulses from the charge division. H8500 circuitry, before digitizing the four signals in the standard DAQ module with integrating ADCs. Energy spectra for six selected 2x2x15mm BGO pixels were recorded using 1500 nsec ADC gate. Energy resolution FWHM @511 keV for each of these pixels is indicated in the table above. During the measurements the BGO array was placed in the center of the PSPMT.





Summary of the pilot BGO Studies with the latest generation large MPPC array

- Energy resolution in the imaging mode with the large 256 MPPC array is approaching 15% FWHM level at 511 keV, equaling what is obtained with H8500 PSPMTs
- MPPC arrays are buttable and do not have the same edge effects as the PSPMTs
- Energy resolution with 4ch readout is the same as with the 16x16 readout
- 2mm pixel separation is excellent at practically any conditions (bias voltage or temperature) also with 4ch readout for the whole module.
- Preliminary study with a thin ~1.6mm pitch array points to a resolution limit of about 1.5mm
- · At lower temperatures performance is better
- Using simple demonstration two-layer DOI stack of shifted 2mm BGO arrays all pixels in both arrays are separated